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EXAMINER	
YUEN, KAN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,296	KINSTLER, GARY A.	
	Examiner	Art Unit	
	KAN YUEN	2464	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11,15-20 and 37-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11,15-20 and 37-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see remark on page 2, filed 11/13/2009, with respect to the rejection(s) of claim(s) 37 and 41 under 112 rejection first paragraph, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

2. Applicant's arguments filed 11/13/2009 have been fully considered but they are not persuasive.

In response to applicant's argument that the NASA Tech Briefs paper provides secondary evidence of non-obviousness, Examiner respectfully disagrees

According to the NASA Tech Brief entitled "Radiation-Tolerant Dual Data Bus" mentioned by the Applicant on page 7, the article generically discusses about using two IEEE 1394b buses that convey identical data signals to carry out redundancy purposes. In case of SEU or latch-up detection, other circumvention circuits would restore correct operation by turning off, then turning back on (remove and reapply power) to the system to reinitializing the affected bus circuitry.

The applicant implies that because the invention was written about in NASA Tech Briefs that the invention would have been non-obvious to a person of ordinary skill in the art at the time of the invention. However, the article, itself, does not evaluate the nonobviousness of the invention. Therefore, the article does not provide sufficient evidence to overcome the current ground of rejection.

3. In response to applicant's arguments against the references (Kramer et al., Fuchs et al. and Gupta et al.) individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

4. In response to applicant's argument on page 4 of the remark, that the reference of Kramer et al. fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Identifying a specific node experiencing letup-up or other single event functional interruption) are not recited in the rejected claim 37. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In addition to claim 37, the applicant argued that the reference of Fuchs does not disclose an architecture that allows a node to clear its own latch-up. The Examiner respectfully disagrees and will further explain the rejection.

According to column 14, lines 35-67, and column 15, 1-30, which states: "When a CPU 32 has failed to re-synchronize after a disagreement and a subsequent resynchronization, a latch-up is detected. Power is then removed and reapplied (recovery command) to the CPU 32 to clear the latch-up." (see column 15, lines 5-12). In other words, the removed and reapplied power causes the CPU to clear its own latch-up. Thus, the CPU can clear it own latch-up when power is reapplied.

The applicant also argued that Fuchs does not teach or suggest an architecture that corrects only the node experiencing latch-up. The Examiner respectfully disagrees and will further explain the rejection.

According to column 14, lines 35-67, and column 15, 1-30, which states: "When a CPU 32 has failed to re-synchronize after a disagreement and a subsequent resynchronization, a latch-up is detected. Power is then removed and reapplied to the CPU 32 to clear the latch-up. From the "power down" state 174, a CPU 32 can be restarted by a power up transition 182 through the disagree-disabled state 186." (see column 15, lines 5-12). In other words, when latch-up of a single CPU is detected, power is removed from the single CPU. From the powered down state 174, the single CPU 32 can be restarted/restored by a power up transition 182 through the disagree-disabled state 186.

Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention implement the recovery command (remove and reapply power) as taught by Fuchs in the network of Kramer et al. The motivation for using the recovery command being that when instability occurs (latch-ups), it provides transmission reliability by shutting off and reapplying power to the system/processor and restore the original function of the system/processor so that circuit stability can be achieved again during or after hazardous environment.

In addition, the Applicant also argued that neither Kramer et al. Fuchs et al. and Gupta et al. disclose the feature for using an alternative bus path to send a recovery command. The Examiner respectfully disagrees and will further explain the rejection.

Gupta et al. from the same or similar fields of endeavor disclosed the feature wherein the recovery command is transmitted via an alternative data bus path (see claim 8, and see fig. 2). Upon detecting of a failure, the redundancy module configured to perform interface line functions for the analog signals (recovery command) transferred via the redundancy bus (alternative bush path). Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the feature as taught by Gupta et al. in the network of Kramer et al. and Fuchs et al. The motivation for using the feature being that it provides redundancy in the network by transmitting control signals such as analog signals (recovery command) in a redundancy bus path.

In addition, the applicant also argued that neither Kramer et al. Fuchs et al. and Gupta et al. disclose the feature for detecting a surge which might indicate latch up (claims 10 and 15). However, according to the previous office action, reference Kim (Pat No.: 6064554) was introduced to teach such limitation.

Thus, the applicant's arguments are not persuasive.

Claim Rejections - 35 USC § 103

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 9, 11, 16, 17, 19, 20, 37-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539) in view of Gupta et al. (Pat No.: 5787070) and further in view of Fuchs et al. (Pat No.: 5923830).

For claim 37, Kramer et al. disclosed the method of periodically transmitting a first message from a first node to a second node on a first line of the serial data bus (column 6, lines 34-60). The central bus subscriber 14 and the active subscriber 16 transmit and/or receive for instance periodically status messages (first message) via the data lines 10, 12;

determining whether the first message was received by the second node (column 6, lines 34-60). The subscribers check whether the status messages were transferred or received within a defined fault tolerance time; and

transmitting a recovery command to the second node if the second node does not respond to the first message (Kramer et al. see column 3, lines 15-35, see column 6, lines 35-67, and see column 7, lines 1-15, and see fig. 1). After fault detection, the transmitting module will generate a relevant message (recovery message) to the module again using any of the 2 buses (10, 12) or the

second bus. Since all bus subscribers transmit message independently, the bus are different. The fault-proof comparator consists of the two homogenous units A0 and B0, the galvanically separated link 96 such as an optical coupler, and relays K1, K2 or a comparable circuit and controls and output level, not described in any detail, in which the power supply of the relevant device or machine or plant is located and which will interrupt (disrupt) the power supply in case the comparator gives the relevant signal, so that the device, machine or plant can be restored in fail-safe state (correct operation).

However, Kramer et al. did not explicitly disclose the feature wherein the recovery command is transmitted via an alternative data bus path; and the recovery command causing the second node to disrupt a monostable condition in the second node and restore functionality of the second node without disrupting the first node and any other nodes of the plurality.

Gupta et al. from the same or similar fields of endeavor disclosed the feature wherein the recovery command is transmitted via an alternative data bus path (Gupta et al. see claim 8, and see fig. 2). Upon detecting of a failure, the redundancy module configured to perform interface line functions for the analog signals (command) transferred via the redundancy bus (alternative data bus) and to distribute corresponding digital signals according to the second communication protocol. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Gupta et al. in the network of Kramer et al. The motivation for using the feature being that it provides redundancy in the network.

Fuchs from the same or similar fields of endeavor disclosed the feature wherein the recovery command causing the second node to disrupt a monostable condition in the second node and restore functionality of the second node without disrupting the first node and any other nodes of the plurality (Fuchs et al. column 14, lines 35-67, column 15, lines 1-10 and see abstract). The CPU 32 are re-synchronized and returned to the "operating, voting enabled state" 156 by transition 196. When a CPU 32 has failed to re-synchronized after a disagreement and a subsequent re-synchronization, a latchup (monostable condition) is suspected. Power is then removed and reapplied to the CPU to clear the latchup. Thus the latchup is disrupted by removing the power from the CPU. Further, according to the abstract, the system logic selects the best chance of recovering from a detected fault by re-synchronizing all CPUs, powering down a faulty CPU, or switching to a spare computer, resetting and re-booting the substituted sole CPU. Therefore, the single substituted CPU is the only CPU that can be re-synchronized without disrupting other CPUs. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Fuchs et al. in the network of Kramer et al. and Gupta et al. The motivation for using the feature being that it provides circuit stability in hazardous environment.

Claim 41 is rejected similar to claim 37.

Regarding claim 38, Kramer et al. disclosed the feature wherein the second node includes a physical layer controller connected (Kramer et al. control modules 56, 58 or 60, 62) to the serial data bus (busses 10, 12) and link layer

controller (Kramer et al. control modules 56, 58 or 60, 62); and wherein a monostable condition is disrupted in at least one of the physical layer controller and the link layer controller (Kramer et al. column 5, lines 10-67, column 6, lines 1-30). Both controller modules 56, 58 in subscriber 18 is monitoring each other for failure (when monostable condition is detected).

Regarding claim 39, Kramer et al. disclosed the feature wherein the link layer controller is coupled to and dc-isolated from the physical layer controller; and wherein disrupting a monostable condition in the link layer controller is independent of disrupting a monostable condition in the physical layer controller (Kramer et al. column 6, lines 1-35). The fault-proof comparator consists of the two homogenous units A0 and B0, the galvanically separated link 96 such as an optical coupler and relays K1, K2. The relays have forced controller contacts, a property where the contacts for the two relay states, i.e. the normally open and the normally closed contacts cannot be opened or closed at the same time, thus they are independent.

Regarding claim 40, Fuchs et al. disclosed the feature wherein the recovery command causes a bus interface circuit operatively connecting the second node to the first bus to be re- initialized (Fuchs et al. column 15, lines 1-10). The CPU 32 are re-synchronized and returned to the "operating, voting enabled state" 156 by transition 196. When a CPU 32 has failed to re-synchronized after a disagreement and a subsequent re-synchronization, a latchup is suspected. Power is then removed and reapplied to the CPU to clear the latchup.

Regarding claim 7, Kramer et al. disclosed the feature wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame (Kramer et al. see column 7, lines 49-55). As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 9, Kramer et al. disclosed the feature wherein determining whether the first message was received includes waiting for a reply from the second node (Kramer et al. column 7, lines 1-30).

Regarding claim 11, Kramer et al. disclosed the feature wherein the second bus is a different type of bus than the serial data bus (Kramer et al. see column 3, lines 15-35) Since all bus subscribers transmit message independently, the bus are different.

Regarding claim 16, Kramer et al. disclosed the feature wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame (Kramer et al. see column 7, lines 49-55). As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 17, Kramer et al. disclosed the feature wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame (Kramer et al. see column 7, lines 49-55). As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 19, Kramer et al. disclosed the feature wherein the second bus is a different type of bus than the first bus (Kramer et al. see column 3, lines 15-35) Since all bus subscribers transmit message independently, the bus are different.

Regarding claim 20, Fuchs et al. disclosed the feature wherein the nodes include a bus interface circuit operatively connected to the serial data bus; and means for receiving the recovery command on the second bus and for re-initializing the bus interface circuit in response to the command (Fuchs et al. column 15, lines 1-10). The CPU 32 are re-synchronized and returned to the "operating, voting enabled state" 156 by transition 196. When a CPU 32 has failed to re-synchronized after a disagreement and a subsequent re-synchronization, a latchup is suspected. Power is then removed and reapplied to the CPU to clear the latchup.

Regarding claim 42, Kramer et al. disclosed the feature wherein the bus interface includes a physical layer controller that is connected to the serial data bus, and a link layer controller that is coupled to and galvanically isolated from the physical layer controller, and wherein a monostable condition in the link layer controller is disrupted independently of a monostable condition in the physical layer controller (Kramer et al. column 6, lines 1-35). The fault-proof comparator consists of the two homogenous units A0 and B0, the galvanically separated link 96 such as an optical coupler and relays K1, K2 and controls an output level, in which the power supply of the relevant device is located and which will interrupt the power supply in case the comparator gives the relevant signal, so that the device can be rendered safe. The relays have forced controller contacts, a property where the contacts for the two relay states, i.e. the normally open and the normally closed contacts cannot be opened or closed at the same time, thus they are independent.

Regarding claim 43, Kramer et al. disclosed the feature wherein each node further includes a second data bus and means for coupling the link layer controller to the second data bus, the means also dc-isolating the link layer controller from the second data bus (Kramer et al. column 4, lines 39-67, column 6, lines 15-35).

Regarding claim 44, Kramer et al. disclosed the feature wherein each node further includes a watchdog timer for monitoring its bus interface (Kramer et al. column 3, lines 1-35).

Regarding claim 45, Fuchs et al. disclosed the feature wherein clearing the latch-up and restoring correct operation includes turning off and then turning back on the bus interface, and also reinitializing affected bus circuitry (Fuchs et al. column 15, lines 1-10). The CPU 32 are re-synchronized and returned to the "operating, voting enabled state" 156 by transition 196. When a CPU 32 has failed to re-synchronized after a disagreement and a subsequent re-synchronization, a latchup is suspected. Power is then removed and reapplied to the CPU to clear the latchup.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539) in view of Gupta et al. (Pat No.: 5787070) and Fuchs et al. (Pat No.: 5923830) as applied to claim 37 above, and further in view of Engels et al. (Pub No.: 2004/0213174).

For claim 8, Kramer et al. Gupta et al. and Fuchs et al. did not disclose the feature wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once each minor frame. Engels et al. from the same or similar fields of endeavor disclosed the feature wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once each minor frame (Engels et al. see paragraph 0028, lines 1-

4). The uplink frame, which includes plurality of mini time slot frames, is allocated for data transmission in each individual slot frame. The data can be any kind of messages. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Engels et al. in the network of Kramer et al. Gupta et al. and Fuchs et al. The motivation for using the feature as taught by Engels et al. in the network of Kramer et al. Gupta et al. and Fuchs et al. being that the minor frames can be transmitted without major delay.

8. Claims 10, 15, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539) in view of Gupta et al. (Pat No.: 5787070) and Fuchs et al. (Pat No.: 5923830) as applied to claim 37 above, and further in view of Kim (Pat No.: 6064554).

For claim 10, Kramer et al. Gupta et al. and Fuchs et al. did not disclose the feature of detecting a current surge in a bus interface circuit operatively connecting the second node to the first bus; and cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit. Kim et al. from the same or similar fields of endeavor disclosed the feature of detecting a current surge in a bus interface circuit operatively connecting the second node to the first bus; and cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit (Kim et al. see column 2, lines 13-40). The power unit is couple to the over-current or current surge detector.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Kim in the network of Kramer et al. Gupta et al. and Fuchs et al. The motivation for using the feature as taught by Kim in the network of Kramer et al. Gupta et al. and Fuchs et al. being that the over-current detection can provide protections to system cause by power outrage.

Regarding claim 15, Kim disclosed the feature wherein the nodes further detect a current surge in the bus interface and report the current surge in the bus interface circuit to the node sending the first message (Kim see column 3, lines 52-67, and see column 4, lines 1-3). As shown, the detected current is transmitting to the USB controller 100.

Regarding claim 18, Kim disclosed the feature wherein each node includes a bus interface circuit operatively connected to the serial data bus; means for detecting a current surge in the bus interface circuit; and means for cycling power to the bus interface circuit in response to detecting the current surge (Kim et al. see column 2, lines 13-40). The power unit is couple to the over-current or current surge detector.

9. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539) in view of Gupta et al. (Pat No.: 5787070) and Fuchs et al. (Pat No.: 5923830) as applied to claim 37 above, and further in view of Groff (Pat No.: 6525436).

For claim 46, Kramer et al. Gupta et al. and Fuchs et al. did not disclose the feature wherein the bus interface is not radiation- hardened. Groff from the same or similar fields of endeavor disclosed the feature wherein the bus interface is not radiation- hardened (Groff column 2, lines 55-65). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Groff in the network of Kramer et al. Gupta et al. and Fuchs et al. The motivation for using the feature being that increases reliability in the system by spacing the interface connected to I/O busses to suppress the emissions of radiation caused by interaction of the device circuit.

Examiner's Note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAN YUEN whose telephone number is (571)270-1413. The examiner can normally be reached on Monday-Friday 10:00a.m-3:00p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky O. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kan Yuen/
Examiner, Art Unit 2464

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2464

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